Remarks

Claims 1-5 and 10-14 currently remain pending. Claims 6-9 were canceled in a previous response. Claims 1-5, 10, 11, and 14 stand rejected. Claim 13 is allowed. Claim 12 stands objected to as being dependent upon a rejected base claim, but is otherwise allowable. No claims are amended herein. The Applicant respectfully traverses the rejections and requests allowance of claims 1-5 and 10-14.

Claim Rejection Under 35 U.S.C. § 102

Claims 1-3, 10, 11, and 14 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent Application Publication No. 2001/0042243 to Fish et al. (hereinafter "Fish"). (Page 2 of the Office action.) The Applicant respectfully disagrees as discussed hereinafter.

Claim 1

Independent computer system claim 1 is reproduced below, with emphasis supplied:

> 1. A computer system having *a plurality of processors* within a cell, the cell comprising:
> a processor type register,
> at least one primary processor;
> a management subprocessor,
> an EEPROM, and
> *mapping hardware coupling the plurality of processors to the EEPROM*;
> wherein at system boot the management subprocessor reads the processor type register to determine an appropriate boot image of *a plurality of boot images recorded within the EEPROM*, and *configures the mapping hardware to map the appropriate boot image into boot address space of the at least one primary processor* of the cell.

The Office action indicates that Fish discloses mapping hardware coupling *a plurality of processors* to an EEPROM, as indicated in claim 1, specifically by way of Figs. 2 and 3, and paragraphs [0017]-[0022] and [0030]-[0031], of Fish. (Page 3 of the Office action.) The Applicant respectfully disagrees, as each of the embodiments of Fish only discloses a single processing unit (PU) 12 (see Figs. 1 and 2) or processor unit 112 (see Figs. 3 and 5). (See also the portions of the detailed description associated with these figures.)

The Office action also indicates that the mapping hardware of claim 1 is shown by way of

gates 108, 109 of Fig. 3. Again, the Applicant respectfully disagrees. The logical gates 108, 109 of Fish are utilized with the embodiment of Fig. 3, which employs separate (i.e., multiple) firmware components 104*a* and 104*b*, unlike the embodiment of Fig. 2, which incorporates a single firmware component 101. (See paragraph [0030].) As the logical gates 108, 109 only turn on or activate one or the other of the firmware components 104*a*, 104*b*, the use of the logical gates 108, 109 of the embodiment of Fig. 3 does not appear to be compatible with the embodiment of Fig. 2, which employs the single firmware component 101 to hold the multiple firmware portions. Instead, in the embodiment of Fig. 3, a cross-reference table 400 contains pointers 410 which are used to indicate which of the common and custom firmware portions of the single firmware component 101 are to be accessed and executed. (See Fig. 4 and paragraphs [0026] and [0027].) As such, Fish does not teach or suggest mapping hardware that maps an appropriate boot image of a plurality of boot images recorded within a single EEPROM into boot address space of a processor, as provided for in claim 1, as Fish does not discuss the use of such hardware with respect to the single firmware component 101 embodiment of Fig. 2. Presumably, the pointers 410 of Fish would be used to direct execution of the appropriate firmware portions without the use of mapping hardware coupling the processor 12 to the firmware component 101 to map the selected firmware portion to a particular boot address space. In fact, booting or initializing of the system apparently occurs in Fish by way of the same common firmware portion 102 being executed for every possible processor, thus likely eliminating the need for such mapping hardware. (See paragraph [0021].)

Thus, based on the foregoing, the Applicant contends that claim 1 is allowable in view of Fish, and such indication is respectfully requested.

Claims 2 and 14

Independent method claim 2 provides, in part, "selecting a compatible boot image from a plurality of boot images, the plurality of boot images contained within an EEPROM," and "configuring mapping hardware to map the compatible boot image of the EEPROM into boot address space of the first processor." Claim 14 incorporates similar provisions.

The Office action employs the logical gates 108, 109 in the rejection of claim 2 using the same rationale as outlined above. (See pages 4 and 6 of the Office action.) Thus, based on the reasons discussed earlier, the Applicant contends that Fish does not teach or suggest configuring

mapping hardware to map a compatible boot image of a plurality of boot images contained within an EEPROM into boot address space of a processor, as provided for in claims 2 and 14, and such indication is respectfully requested.

Claims 3, 10, and 11

Claims 3, 10, and 11 depend from independent claim 2, thus incorporating the provisions of that claim. Therefore, the Applicant asserts that claims 3, 10, and 11 are allowable for at least the same reasons set forth above in support of claim 2, and such indication is respectfully requested.

Therefore, in light of the foregoing, the Applicant respectfully requests withdrawal of the 35 U.S.C. § 102 rejection of claims 1-3, 10, 11, and 14.

Claim Rejection Under 35 U.S.C. § 103

Claims 4 and 5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fish in view of U.S. Patent No. 6,748,526 to Thangadurai. (Page 7 of the Office action.) Claims 4 and 5 depend from claim 2, and thus include the provisions of that claim. Thus, the Applicant contends that claims 4 and 5 are allowable for at least the reasons presented above in support of claim 2, and therefore respectfully requests withdrawal of the 35 U.S.C. § 103(a) rejection of claims 4 and 5.

Indication of Allowable Subject Matter

According to the Office action, "[c]laim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims." (Page 7 of the Office action.) As indicated above, the Applicant contends that claim 11, from which claim 12 depends, is allowable in light of the discussion presented earlier. Thus, the Applicant asserts that claim 12 is allowable in its present form, and such indication is respectfully requested.

Claim 13 is allowed. (Id.) Thus, the allowability of claim 13 is not discussed further herein. The Applicant thanks the Examiner for his consideration of this claim.

Conclusion

Based on the above remarks, the Applicant submits that claims 1-5 and 10-14 are allowable. Other reasons in favor of patentability exist, but such reasons are omitted in the interests of clarity and brevity. The Applicant thus respectfully requests allowance of claims 1-5 and 10-14.

The Applicant believes no fees are due with respect to this filing. However, should the Office determine additional fees are necessary, the Office is hereby authorized to charge Deposit Account No. 08-2025 accordingly.

Respectfully submitted,

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/Kyle J. Way/

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